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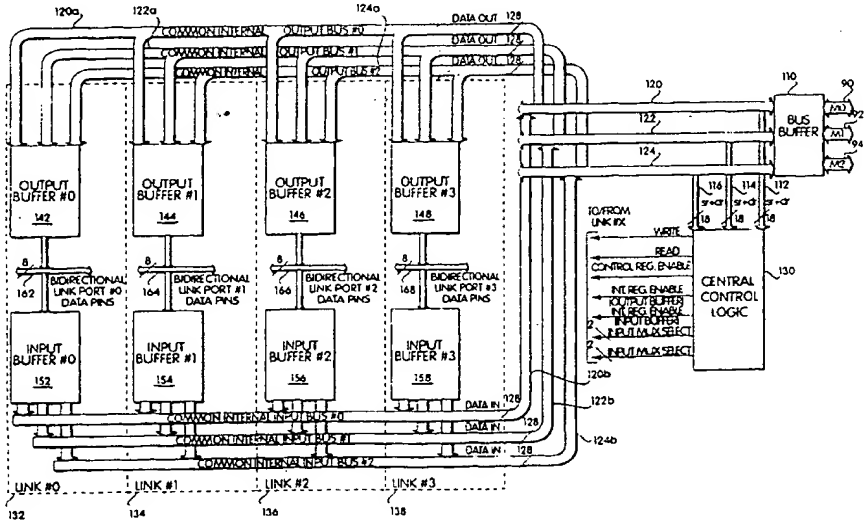

(57) Abstract

A high performance digital signal processor includes a bidirectional communication port for communication with an external device. The bidirectional communication port includes a first transmitting circuit for transmitting to the external device a first clock on a first control line in a transmit mode and for transmitting data words on plural data lines in synchronism with the first clock, and a first receiving circuit for receiving a first acknowledge signal on a second control line in the transmit mode. The communication port further includes a second receiving circuit for receiving a second clock on the second control line in a receive mode and for receiving data words on the data lines in synchronism with the second clock, and a second transmitting circuit for transmitting a second acknowledge signal on the first control line in the receive mode. The communication port further includes switching means for switching between the transmit mode and the receive mode.

BIDIRECTIONAL COMMUNICATION PORT FOR DIGITAL SIGNAL PROCESSOR

Field of the Invention

This invention relates to digital signal processors and, more particularly, to a bidirectional communication port for high speed, point-to-point communication between digital signal processors, and between digital signal processors and external devices.

Background of the Invention

A digital signal computer, or digital signal processor (DSP), is a special purpose computer that is designed to optimize performance for digital signal processing applications, such as, for example, fast Fourier transforms, digital filters, image processing and speech recognition. Digital signal processor applications are typically characterized by real time operation, high interrupt rates and intensive numeric computations. In addition, digital signal processor applications tend to be intensive in memory access operations and to require the input and output of large quantities of data. Thus, designs of digital signal processors may be quite different from those of general purpose computers.

One approach that has been used in the architecture of digital signal processors to achieve high speed numeric computation is the Harvard architecture, which utilizes separate, independent program and data memories so that the two memories may be accessed simultaneously. This architecture permits an instruction and an operand to be fetched from memory in a single clock cycle. Current architectures integrate the computation unit and the memory on a single integrated circuit, or chip, to provide a self-contained, high performance digital signal processor.

One important aspect of DSP chips is external communication. Because the DSP processes the large quantities of data, it is necessary to transfer data to and from the internal memory and the computation unit of the DSP chip efficiently and at high speed. The DSP chip typically includes a parallel external bus for communicating with a host computer, an external memory and other external devices such as, for example, an analog-to-digital converter. The external bus may also be used to interconnect two or more DSP chips in a multiprocessor configuration, or cluster, for increased computational capability. The bus

transmit mode. The bidirectional communication port further comprises second receiving means for receiving a second clock on the second control line in a receive mode and for receiving data words on the plural data lines in synchronism with the second clock, and second transmitting means for transmitting a second acknowledge signal on the first control line in the receive mode. The communication port further comprises switching means for switching between the transmit mode and the receive mode. The communication port may be used for high speed communication between digital signal processors or for communication between a digital signal processor and an external device.

In one embodiment, the first transmitting means includes means for transmitting data words of m bits each, each of the data words being transmitted on 8 data lines as a series of m/8 bytes. The second receiving means includes means for receiving data words of m bits each, and each of the data words is received on the 8 data lines as a series of m/8 bytes.

The switching means may include means for asserting the first clock in the receive mode to thereby generate a transmit request to switch from the receive mode to the transmit mode. The switching means may further include means responsive to assertion of the second clock in the transmit mode for switching from the transmit mode to the receive mode.

The first transmitting means may include means for transmitting a verification byte following the transmission of a predetermined number of data bytes. The verification byte may comprise a checksum byte. The second receiving means may comprise means for receiving a verification byte following a predetermined number of received data bytes and means responsive to the verification byte for detecting an error in the received data byes.

The first receiving means may include means responsive to a transition in the first acknowledge signal during transmission of a data word for confirming connection of the communication port to the external device. The first receiving means may further include means responsive to deassertion of the first acknowledge signal for a timeout period for indicating a fault condition. The second receiving means may include means responsive to an unchanging state of the second clock for a predetermined time for indicating a fault condition.

The bidirectional communication port may include a third control line. In one configuration, the third control line indicates the direction of transmission of the communication port. In another configuration, the third control line is used for frame synchronization.

According to another aspect of the invention, a method for bidirectional

controller 30, an instruction alignment buffer (IAB) 32 and a primary instruction decoder 34. The computation blocks 12 and 14, the instruction alignment buffer 32, the primary instruction decoder 34 and the control block 24 constitute a core processor which performs the main computation and data processing functions of the DSP 10. The external port 28 controls external communications via an external address bus 58 and an external data bus 68. The link ports 26 control external communication via communication ports 36. The DSP is preferably configured as a single monolithic integrated circuit and is preferably fabricated using a 0.35 micron gate, four metal, SRAM CMOS process. In a preferred embodiment, an external clock (not shown) at a frequency of 41.5 MHz is internally multiplied by four to provide an internal clock at 166 MHz.

The memory 16 includes three independent, large capacity memory banks 40, 42 and 44. In a preferred embodiment, each of the memory banks 40, 42 and 44 has a capacity of 64K words of 32 bits each. As discussed below, each of the memory banks 40, 42 and 44 preferably has a 128 bit data bus. Up to four consecutive aligned data words of 32 bits each can be transferred to or from each memory bank in a single clock cycle.

The elements of the DSP 10 are interconnected by buses for efficient, high speed operation. Each of the buses includes multiple lines for parallel transfer of binary information. A first address bus 50 (MA0) interconnects memory bank 40 (M0) and control block 24. A second address bus 52 (MA1) interconnects memory bank 42 (M1) and control block 24. A third address bus 54 (MA2) interconnects memory bank 44 (M2) and control block 24. Each of the address buses 50, 52 and 54 is preferably 16 bits wide. An external address bus 56 (MAE) interconnects external port 28 and control block 24. The external address bus 56 is interconnected through external port 28 to external address bus 58. Each of the external address buses 56 and 58 is preferably 32 bits wide. A first data bus 60 (MD0) interconnects memory bank 40, computation blocks 12 and 14, control block 24, link ports 26, IAB 32 and external port 28. A second data bus 62 (MD1) interconnects memory bank 42, computation blocks 12 and 14, control block 24, link ports 26, IAB 32 and external port 28. A third data bus 64 (MD2) interconnects memory bank 44, computation blocks 12 and 14, control block 24, link ports 26, IAB 32 and external port 28. The data buses 60, 62 and 64 are connected through external port 28 to external data bus 68. Each of the data buses 60, 62 and 64 is preferably 128 bits wide, and external data bus 68 is preferably 64 bits wide.

The first address bus 50 and the first data bus 60 comprise a bus for transfer of data to

memory (not shown) via external port 28. The desired external memory address is placed on address bus 56. The external address is coupled through external port 28 to external address bus 58. The external memory supplies the requested data word or data words on external data bus 68. The external data is supplied via external port 28 and one of the data buses 60, 62 and 64 to one or both of computation blocks 12 and 14. The DRAM controller 30 controls the external memory.

As indicated above, each of the memory banks 40, 42 and 44 preferably has a capacity of 64k words of 32 bits each. Each memory bank may be connected to a data bus that is 128 bits wide. In an alternative embodiment, each data bus may be 64 bits wide, and 64 bits are transferred on each of clock phase 1 and clock phase 2, thus providing an effective bus width of 128 bits. Multiple data words can be accessed in each memory bank in a single clock cycle. Specifically, data can be accessed as single, dual or quad words of 32 bits each. Dual and quad accesses require the data to be aligned in memory. Typical applications for quad data accesses are the fast Fourier transform (FFT) and complex FIR filters. Quad accesses also assist double precision operations. Preferably, instructions are accessed as quad words. However, as discussed below, instructions are not required to be aligned in memory.

Using quad word transfers, four instructions and eight operands, each of 32 bits, can be supplied to the computation blocks 12 and 14 in a single clock cycle. The number of data words transferred and the computation block or blocks to which the data words are transferred are selected by control bits in the instruction. The single, dual, or quad data words can be transferred to computation block 12, to computation block 14, or to both. Dual and quad data word accesses improve the performance of the DSP 10 in many applications by allowing several operands to be transferred to the computation blocks 12 and 14 in a single clock cycle. The ability to access multiple instructions in each clock cycle allows multiple operations to be executed in each cycle, thereby improving performance. If operands can be supplied faster than they are needed by the computation blocks 12 and 14, then there are memory cycles left over that can be used by the DMA address generators 76 and 78 to provide new data to the memory banks 40, 42 and 44 during those unused cycles, without stealing cycles from the core processor. Finally, the ability to access multiple data words makes it possible to utilize two or more computation blocks and to keep them supplied with operands. The ability to access single or dual data words reduces power consumption in comparison with a configuration where only quad data words are accessed.

A preferred protocol for bidirectional data transmission is described with reference to FIG. 3 and the timing diagram of FIG. 4. The control lines LxCLKA and LxCLKB form a handshake pair that permits asynchronous data transfers, wherein the transmitter provides a clock, or strobe, on one clock line, and the receiver provides an Acknowledge signal on the other clock line. One control line is assigned to each digital signal processor. A digital signal processor drives one control line and receives on the other control line. When the DSP is transmitting, the control line is driven as a strobe. When the DSP is receiving, the same control line is driven as an Acknowledge signal.

In the example of FIGS. 3 and 4, a 32-bit word transmitted by the link port includes 4 bytes, and a quad word includes 16 bytes. As shown in FIG. 4, two bytes are transmitted on each clock cycle. Both the rising and falling edges of the clock are used to transmit data. A first byte is transmitted on the 8 data lines on the rising edge of the clock, and a second byte is transmitted on the falling edge of the clock. The receiver asserts the Acknowledge signal when it is ready to accept another word in its receive buffer. The transmitter samples the Acknowledge signal near the end of each quad word transmission, i.e., after every 16 bytes. If the Acknowledge signal is deasserted at that time, the transmitter does not transmit a new word. When the Acknowledge signal is eventually asserted again, the transmitter waits 4 cycles, as described below, to be sure that the receiver has not changed transmission direction. Then, the transmitter begins transmission of the next quad word. When the transmit buffer is empty, the clock signal remains high until the buffer is refilled, regardless of the state of the Acknowledge signal.

The link ports permit bidirectional communication in which the data transfer direction may change. The programmer has control of the packet size of the data transmitted before the receiver may request a change of transmission direction. In one example, a 256 word packet or an infinite size packet may be selected. When the 256 word packet is selected, the transmission direction may change after 256 words have been transmitted. When an infinite size packet is selected, the transmitter continues transmitting until it is finished.

When a link port is currently receiving and has data to transmit, i.e., it wants to change direction, it deasserts its Acknowledge signal after a packet of the selected packet size, as indicated by a received word counter, has been received. When the transmitter stops transmitting at the end of the quad word, the receiver can switch to transmit mode and begin transmitting data by using its LxCLK line for sending a strobe instead of the Acknowledge

configuration, the LxDIR line indicates the direction of transmission of the link port. The direction control signal may be utilized when a driver circuit external to the DSP chip is used, for example, to transmit over relatively long distances or to transmit on optical fibers. The state of the direction control signal indicates the direction of transmission.

In a second configuration, the LxDIR line is used for frame synchronization in multiple channel transmission. In the receive mode, the frame synch signal may be asserted low to signify an end of frame/buffer. The frame synch signal is sampled on the link clock rising edge at the end of a quad word. The transition from logic "1" to logic "0" signifies end of buffer. This is interpreted as meaning that the bytes that have been received thus far, including the last one, are the complete buffer. In the transmit mode, the frame synch signal signifies end of buffer and is asserted low just prior to the last byte of the current DMA being driven on the link port. The transmit frame synch signal is deasserted high when a new DMA block begins transmitting.

Block diagrams of output buffer 142 and input buffer 152 of link port 132 are shown in FIG. 5. A selected one of output buses 120a, 122a and 124a is connected by an output bus multiplexer 220 to an internal register 222. The outputs of internal register 222 are connected to inputs of an external register 224. The outputs of external register 224 connected through transmit control logic 230 to data path 162. The LxCLKA and LxCLKB control lines are connected to transmit control logic 230. An output multiplexer 234 selects control lines for the appropriate bus and provides the selected control lines to transmit control logic 230.

In input buffer 152, data path 162 is coupled through receive control logic 250 to an external register 252. The outputs of external register 252 are coupled to inputs of an internal register 254, and the outputs of internal register 254 are coupled to an input bus multiplexer 256. The input bus multiplexer 256 couples the outputs of internal register 254 to a selected one of input buses 120b, 122b and 124b. An input multiplexer 260 selects control signals and provides the selected control signals to receive control logic 250. The LxCLKA and LxCLKB control lines are connected to receive control logic 250. A control register 262 contains control information for controlling the operation of the input and output buffers.

When the link port is transmitting, internal register 222 accepts internal memory data or DMA data. External register 224 performs unpacking of the quad data word into bytes, with the most significant byte first. Registers 222 and 224 form a two-stage first-in first-out buffer (FIFO). Two writes can be made to the buffer by the internal memory or the DMA

unit 460. The error unit 450 generates a local verification byte from the received data bytes and compares the local verification byte with the received verification byte to determine an error condition, as described below.

Thus far, the bidirectional link ports of the present invention have been described in connection with point-to-point communication, wherein one device is connected to each end of a communication channel. According to a further feature of the invention, the link ports of three or more devices may be connected in a bus configuration. The bus configuration of the bidirectional link ports may operate in a point-to-point mode, wherein one digital signal processor connected to the bus transmits and another device receives, all other devices connected to the bus being tristated. In a broadcast mode, one digital signal processor broadcasts data to the other devices connected to the link port bus. In the broadcast mode, the Acknowledge signals are wire-ored so that any device connected to the bus can deassert the Acknowledge signal. When the link ports are used in a bus configuration, communication between devices over the external bus 58, 68 (FIG. 1) is necessary to establish which device on the link port bus is transmitting and which device or devices are receiving.

According to another feature of the invention, the link ports may operate in a flow-through configuration. Referring again to FIG. 2, data may, for example, be received by link port 132 from one external device and may be passed to link port 134 for transmission to a second external device. In particular, the data received on data path 162 is transferred from input buffer 152 of link port 132 to output buffer 144 of link port 134 for transmission on data path 164.

According to a further feature of the invention, the link ports may be used for DMA transfers to and from the internal memory 16 (FIG. 1) of the DSP or for DMA transfers to and from external memory via the external bus 58, 68. The bidirectional link ports of the present invention may include one or more error detection features. In a first error detection feature, a verification byte may be transmitted following a predetermined number of data bytes. For example, a verification byte may be transmitted following each quad word of 16 bytes. The verification byte may be calculated based on the data bytes transmitted using a conventional checksum calculation. The receiver makes the same calculation on the received data bytes and generates a local verification byte. The local verification byte is compared with the received verification byte. If the local verification byte does not match the received verification byte, an error condition is indicated. The receiver may generate an exception

introduced on successive training bytes until an error occurs. The correct timing may be established as the center of the range between positive and negative timing delays which produce errors. The correct delay is used for receipt of data bytes. The training sequence may be repeated as often as desired.

Operation of the control unit 460 (FIG. 8) in the receive control logic 250 is described with reference to the flow chart of FIGS. 9A and 9B. In the following, the link port is described as having a transmitter and a receiver, one of which has control of the link port. If the receiver is determined to be enabled in step 510, the programmed transfer speed is checked in step 512 and is changed as necessary in step 514 or 516. If the transmitter is the dominator (has control of the link port), as determined in step 520, the receiver waits. Otherwise, the receiver buffers are set in step 522 and a determination is made in step 524 as to whether the control register 262 or the input buffer internal register 254 has been accessed by another resource. If the control register or the input buffer internal register has been accessed, the appropriate select signal is sent to the control logic in step 526. If a receiver problem is detected in step 530, the Acknowledge signal is deasserted in step 532 and further operation is terminated. If a receiver problem is not detected, the Acknowledge signal is asserted in step 534. The receiver then looks for an active clock input in step 536. When an active clock input is detected, the byte on data path 162 is latched into external register 252 (FIG. 5) in step 540. In step 542, a determination is made as to whether 16 bytes have been received. When 16 bytes have not been received, the process returns to step 524 to receive additional bytes. After 16 bytes have been received, the process proceeds to step 550 (FIG. 9B) for processing of the verification byte. If an active clock input is not detected in step 536, a determination is made in step 546 as to whether a prescribed timeout period has elapsed. If the timeout period has not elapsed, the process returns to step 536 to look for an active clock input. After the timeout period has elapsed, a connectivity error interrupt is generated in step 548.

Referring now to FIG. 9B, a local verification byte is compared to the received verification byte in step 550 and the internal register is clocked in step 552. A determination is made in step 554 as to whether the DMA or interrupt is enabled. When the DMA is enabled, a DMA request signal, DMAR, is sent to the DMA controller in step 556. When the interrupt is enabled, an interrupt request signal is generated in step 558. In step 560, the receive status is sent to control register 262. In step 562, the Acknowledge signal is

632. Otherwise, the transmitter determines in step 634 whether the Acknowledge signal is asserted.

When the Acknowledge signal is asserted, a determination is made in step 640 as to whether any data is available for transmission. If data is not available for transmission, the clock signal is kept at a high level in step 642. In step 644, a determination is made as to whether a time equal to four clock cycles has elapsed. When four clock cycles have not elapsed, the process returns to step 634. After four clock cycles have elapsed, the process proceeds to step 626. When data is available for transmission in step 640, the clock signal is asserted in step 652, thereby transmitting a byte on the data lines. Then, a determination is made in step 654 as to whether 16 bytes have been transmitted. When 16 bytes have not been transmitted, the process returns to step 626 for transmission of the next byte in the quad word. When the 16 byte quad word has been transmitted, the process proceeds to step 660 (see FIG. 10B).

When the Acknowledge signal is not asserted, as determined in 634, the data lines are left in the present state in step 636. Then, a determination is made in step 646 as to whether transitions are present on the Acknowledge line. When transitions are present on the Acknowledge line, the process proceeds to step 650 for changing to the receive mode. When transitions are not present on the acknowledge line, as determined in step 646, a determination is made in step 648 as to whether a predetermined timeout period has elapsed. When the timeout period has not elapsed, the process returns to step 634. When the timeout period has elapsed, as determined in step 648, an error interrupt is generated.

Referring now to FIG. 10B, a verification byte is transmitted in step 660 and connectivity is checked in step 662 by determining whether the Acknowledge signal from the receiver has been deasserted during the transmission of the quad data word. In step 664, a determination is made as to whether a new data word is available in internal register 222 for transmission. When a new data word is present in internal register 222, the new word is moved to the external register 224 in step 666, and the DMA request signal, DMAR, is sent to the DMA controller in step 668 if DMA is enabled. The transmit status is then sent to control register 262 in step 670. In step 672, a determination is made as to whether transitions are present on the Acknowledge line. When transitions are present on the Acknowledge line, the dominator line is changed to indicate the receive mode in step 650, and a four clock cycle delay is initiated in step 676. Following the four clock cycle delay, the process returns to step

CLAIMS

What is claimed is:

1. In a digital signal processor, a bidirectional communication port for communication with an external device, said bidirectional communication port comprising:

first transmitting means for transmitting to the external device a first clock on a first control line in a transmit mode and for transmitting to the external device data words on plural data lines in synchronism with said first clock;

first receiving means for receiving from the external device a first acknowledge signal on a second control line in the transmit mode;

second receiving means for receiving a second clock on the second control line in a receive mode and for receiving from the external device data words on said plural data lines in synchronism with said second clock;

second transmitting means for transmitting a second acknowledge signal on said first control line in the receive mode; and

switching means for switching between the transmit mode and the receive mode.

2. A bidirectional communication port as defined in claim 1 wherein said first transmitting means includes means for transmitting data words of m bits each, said data words being transmitted on n data lines as a series of m/n nibbles of n bits each, where n is at least 4, and wherein said second receiving means includes means for receiving data words of m bits each on said n data lines as a series of m/n nibbles of n bits each.

3. A bidirectional communication port as defined in claim 2 wherein said data words are received on 8 data lines.

4. A bidirectional communication port as defined in claim 1 wherein said first transmitting means includes means for transmitting data words of m bits each, each of said data words being transmitted on said data lines as a series of m/8 bytes and wherein said second receiving means includes means for receiving data words of m bits each, each of said

means further includes means for counting received data words in the receive mode and wherein said means for asserting said first clock generates said transmit request when a predetermined number of data words have been received.

13. A bidirectional communication port as defined in claim 1 wherein said switching means includes means responsive to assertion of said second clock in the transmit mode for switching from the transmit mode to the receive mode.

14. A bidirectional communication port as defined in claim 4 wherein said first transmitting means includes means for transmitting a verification byte following transmission of a predetermined number of data bytes.

15. A bidirectional communication port as defined in claim 4 wherein said second receiving means includes means for receiving a verification byte following receipt of a predetermined number of data bytes and means for comparing the received verification byte with a calculated verification byte to thereby identify an error condition.

16. A bidirectional communication port as defined in claim 1 wherein said first receiving means includes means responsive to a transition in said first acknowledge signal during transmission of a data word for confirming connection of said communication port to the external device.

17. A bidirectional communication port as defined in claim 1 wherein said first receiving means includes means responsive to deassertion of said first acknowledge signal for a timeout period for indicating an error condition.

18. A bidirectional communication port as defined in claim 1 wherein said second receiving means includes means responsive to an unchanging state of the second clock for a predetermined time for indicating an error condition.

19. A bidirectional communication port as defined in claim 1 further comprising means for asserting a third control line indicative of transmission direction.

24. A digital signal processor as defined in claim 23, wherein said transmit buffer includes means for unpacking the data words for transmission of bytes on said data lines in the transmit mode and wherein said receive buffer includes means for packing bytes of the data words received on said data lines in the receive mode.

25. A digital signal processor as defined in claim 21, wherein said first receiving means includes means for sampling said first acknowledge signal near the end of transmission of a predetermined number of said data words and for transmitting the next data word when said first acknowledge signal is asserted.

26. A digital signal processor as defined in claim 21, wherein said switching means includes means for asserting said first clock in the receive mode to thereby generate a transmit request to switch from the receive mode to the transmit mode.

27. A digital signal processor as defined in claim 21, wherein said switching means includes means responsive to assertion of said second clock in the transmit mode for switching from the transmit mode to the receive mode.

28. A digital signal processor as defined in claim 22, wherein said first transmitting means includes means for transmitting a verification byte following transmission of a predetermined number of data bytes.

29. A digital signal processor as defined in claim 22, wherein said second receiving means includes means for receiving a verification byte following receipt of a predetermined number of data bytes and means for comparing the received verification byte with a calculated verification byte to thereby identify an error condition.

30. A digital signal processor as defined in claim 21, wherein said first receiving means includes means responsive to a transition in said first acknowledge signal during transmission of a data word for confirming connection of said communication port to the external device.

31. A digital signal processor as defined in claim 21, wherein said first receiving means

plural data lines in synchronism with said second clock; and

(d) said digital signal processor transmitting a second acknowledge signal on said first control line in the receive mode.

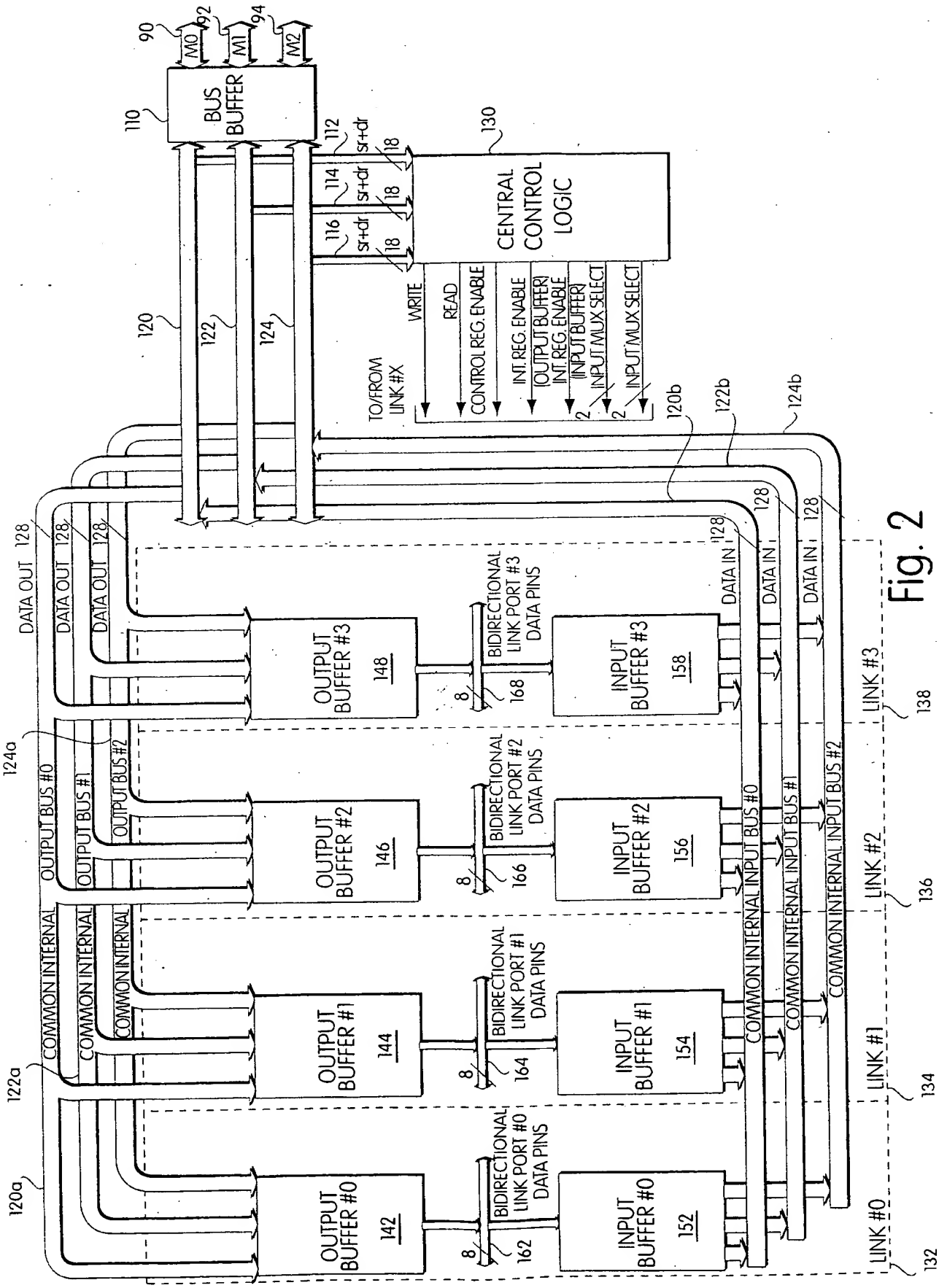
BUS BUFFER
CENTRAL CONTROL LOGIC
WRITE
READ
CONTROL REG. ENABLE
INT. REG. ENABLE (OUTPUT BUFFER)
INT. REG. ENABLE (INPUT BUFFER)
INPUT MUX SELECT
INPUT MUX SELECT
TO/FROM LINK #X
OUTPUT BUFFER #3
OUTPUT BUFFER #2
OUTPUT BUFFER #1
OUTPUT BUFFER #0
INPUT BUFFER #3
INPUT BUFFER #2
INPUT BUFFER #1
INPUT BUFFER #0
BIDIRECTIONAL LINK PORT #3 DATA PINS
BIDIRECTIONAL LINK PORT #2 DATA PINS
BIDIRECTIONAL LINK PORT #1 DATA PINS
BIDIRECTIONAL LINK PORT #0 DATA PINS
DATA OUT
DATA IN
OUTPUT BUS #0
OUTPUT BUS #1
OUTPUT BUS #2
COMMON INTERNAL
COMMON INTERNAL INPUT BUS #0
COMMON INTERNAL INPUT BUS #1
COMMON INTERNAL INPUT BUS #2
LINK #3
LINK #2
LINK #1
LINK #0

Fig. 2

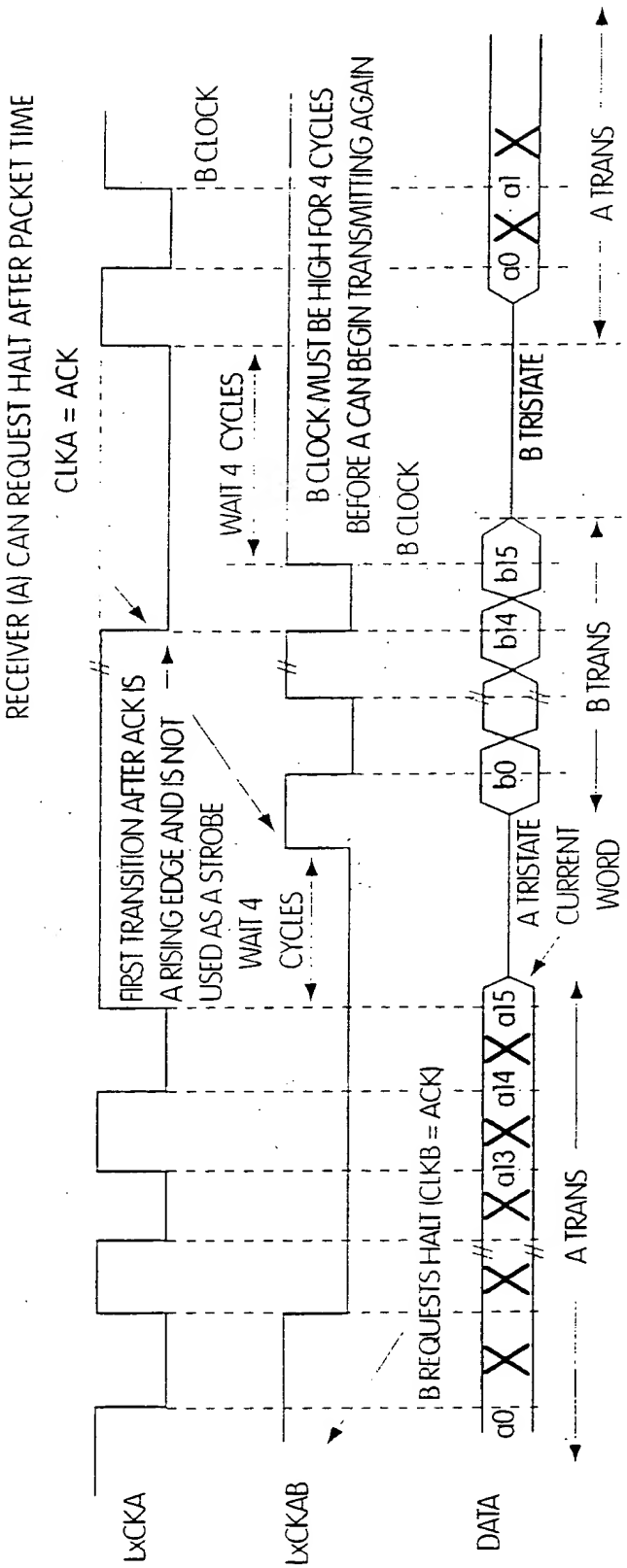
RECEIVER (A) CAN REQUEST HALT AFTER PACKET TIME
CLKA = ACK
B CLOCK
WAIT 4 CYCLES
B CLOCK MUST BE HIGH FOR 4 CYCLES
BEFORE A CAN BEGIN TRANSMITTING AGAIN
B CLOCK
B TRISTATE
A TRANS
FIRST TRANSITION AFTER ACK IS
A RISING EDGE AND IS NOT
USED AS A STROBE
WAIT 4
CYCLES
B TRANS
A TRISTATE
CURRENT
WORD
COMPLETED
B REQUESTS HALT (CLKB = ACK)
A TRANS
LxCKA
LxCKAB
DATA
a0
a13
a14
a15
b0
b14
b15
a0
a1

Fig. 4

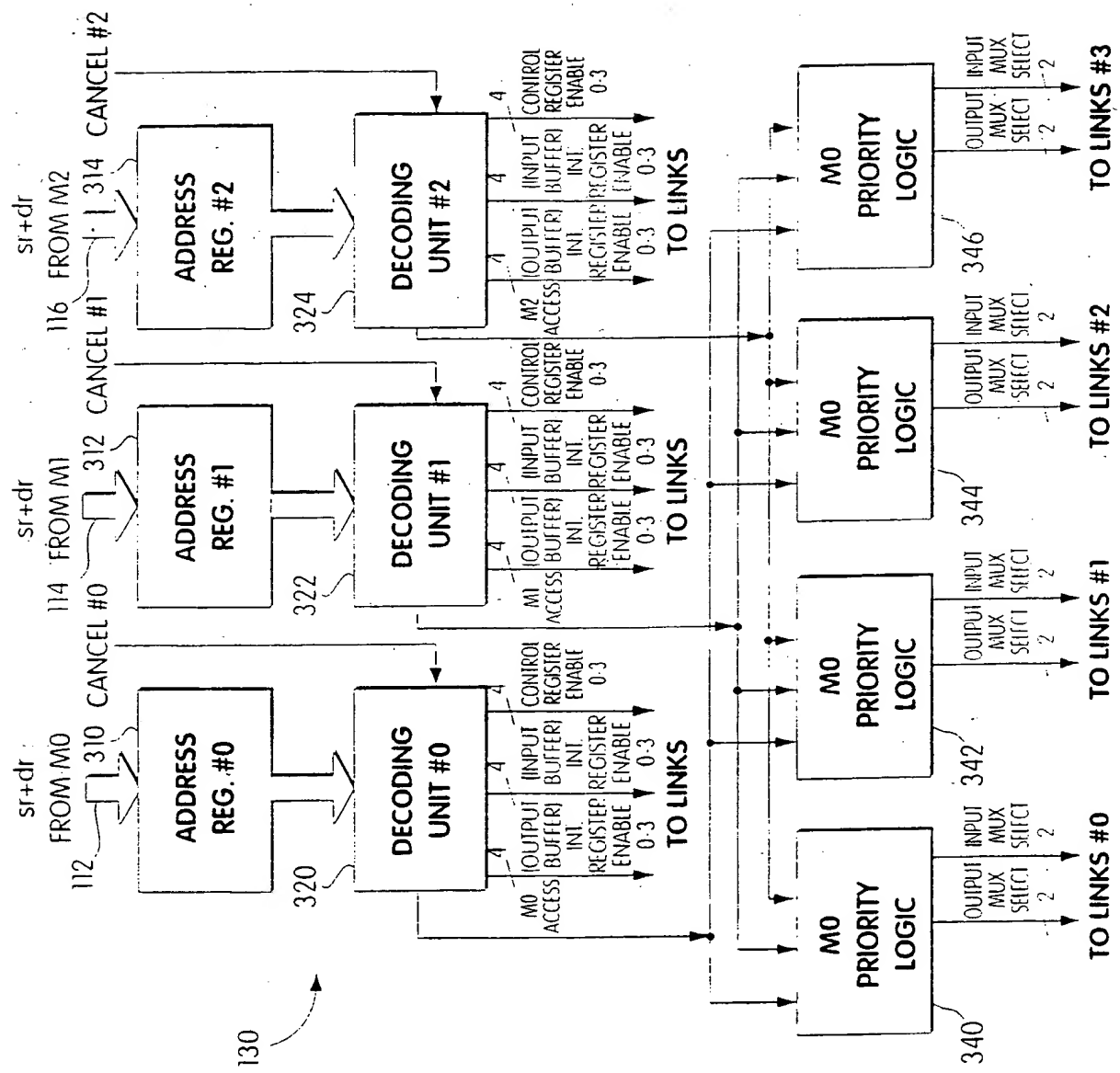
sr+dr FROM M0
112
310
CANCEL #0
ADDRESS REG. #0
320
DECODING UNIT #0
sr+dr FROM M1
114
312
CANCEL #1
ADDRESS REG. #1
322
DECODING UNIT #1
sr+dr FROM M2
116
314
CANCEL #2
ADDRESS REG. #2
324
DECODING UNIT #2
M0 ACCESS
M1 ACCESS
M2 ACCESS
OUTPUT BUFFER/ INT. REGISTER ENABLE 0:3
INPUT BUFFER/ INT. REGISTER ENABLE 0:3
CONTROL REGISTER ENABLE 0:3
TO LINKS
M0 PRIORITY LOGIC
340
342
344
346
OUTPUT MUX SELECT 2
INPUT MUX SELECT 2
TO LINKS #0
TO LINKS #1
TO LINKS #2
TO LINKS #3
130

Fig. 6

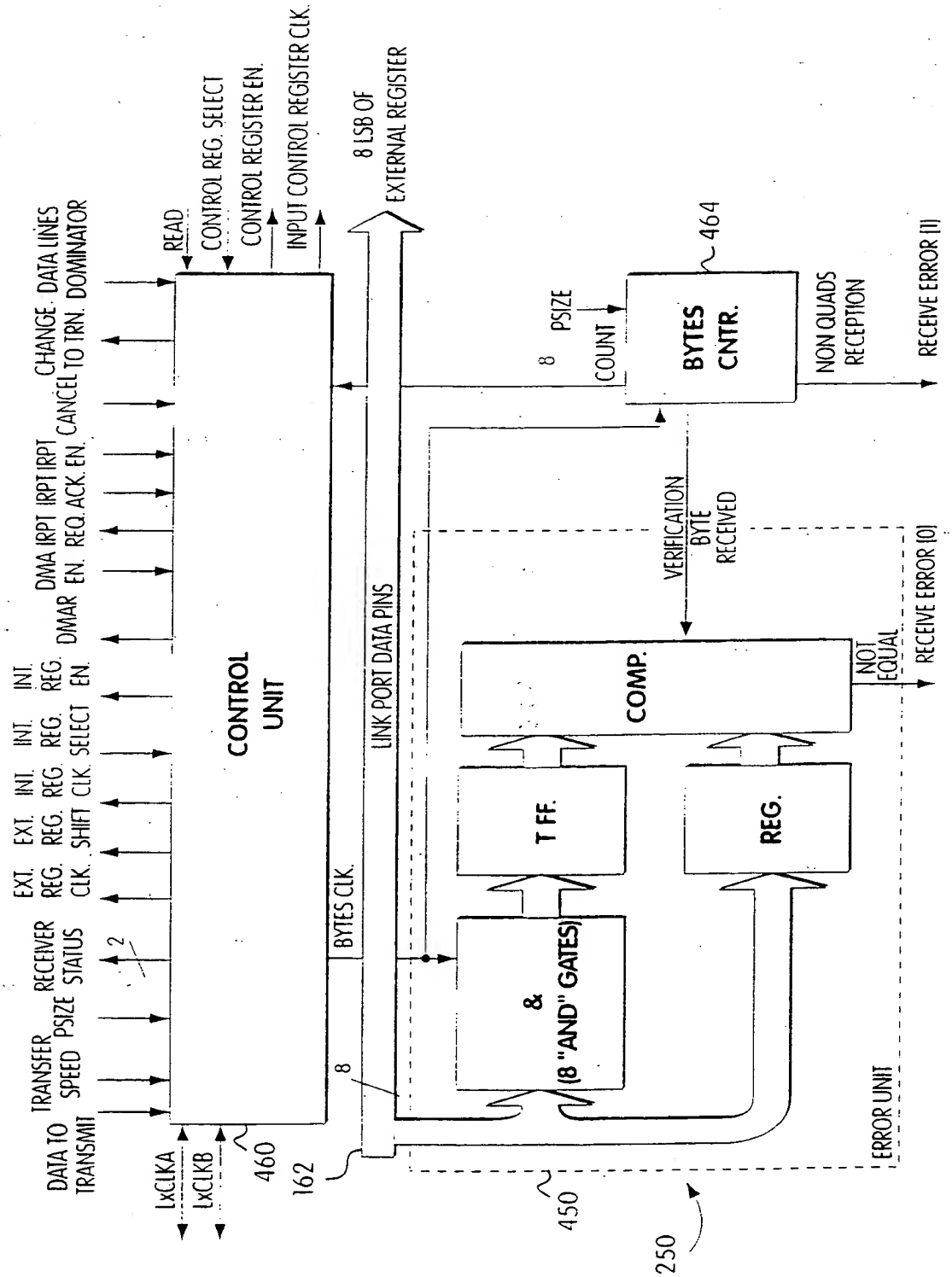
DATA TO TRANSMIT
TRANSFER SPEED
PSIZE
RECEIVER STATUS
2
EXT. REG. CLK.
EXT. REG. SHIFT CLK.
INT. REG. CLK.
INT. REG. SELECT
INT. REG. EN.
DMAR
DMA IRPT EN.
IRPT REQ.
IRPT ACK. EN.
CANCEL
CHANGE. DATA LINES TO TRN. DOMINATOR
READ
CONTROL REG. SELECT
CONTROL REGISTER EN.
INPUT CONTROL REGISTER CLK.
8 LSB OF EXTERNAL REGISTER
CONTROL UNIT
LxCLKA
LxCLKB
460
162
BYTES CLK.
8
LINK PORT DATA PINS
8
PSIZE
COUNT
464
BYTES CNTR.
NON QUADS RECEPTION
RECEIVE ERROR (1)
VERIFICATION
BYTE RECEIVED
COMP.
NOT EQUAL
RECEIVE ERROR (0)
T FF.
REG.
&
(8 "AND" GATES)
ERROR UNIT
450
250

Fig.8

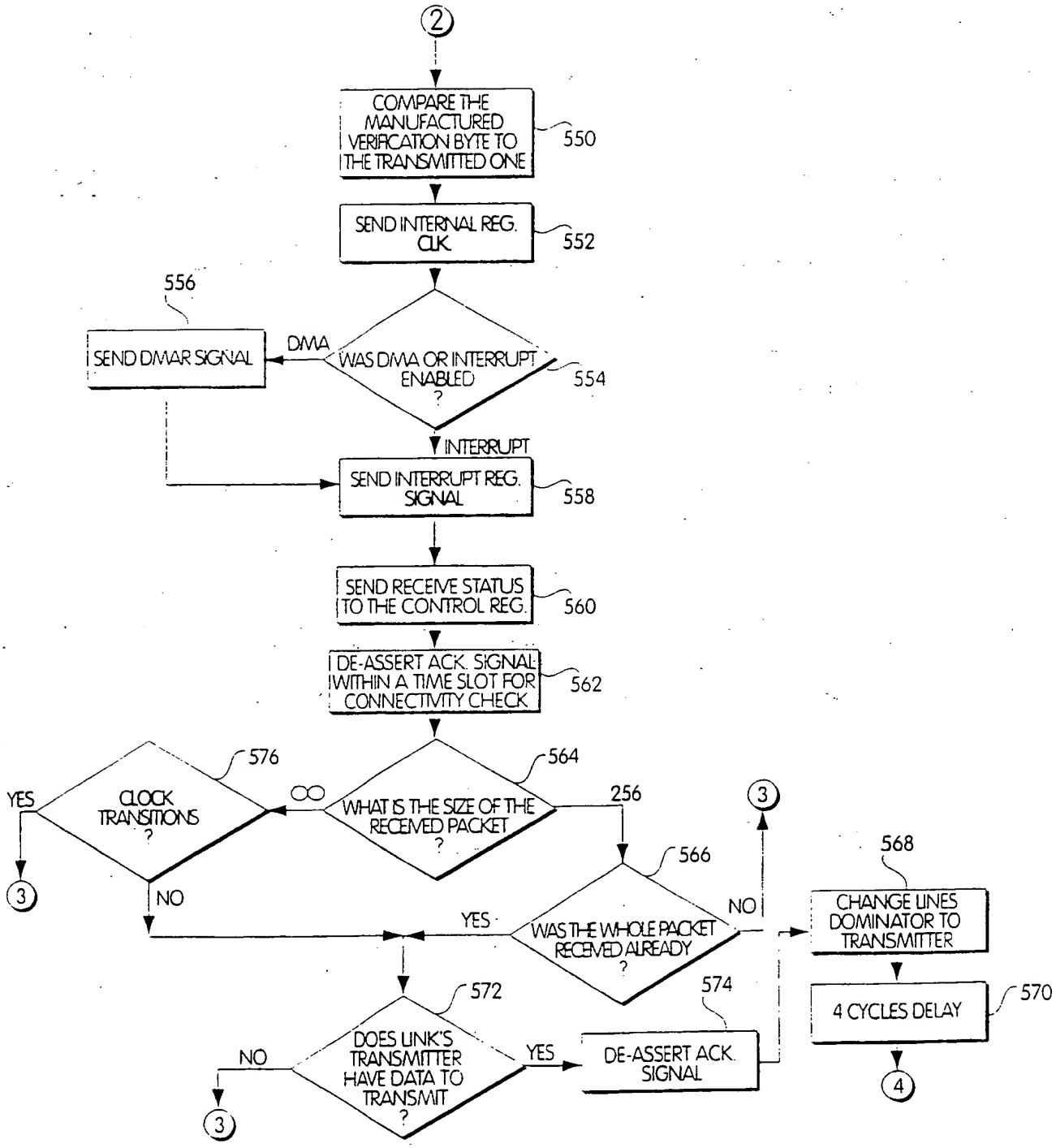
2
COMPARE THE MANUFACTURED VERIFICATION BYTE TO THE TRANSMITTED ONE
550
SEND INTERNAL REG. CLK
552
556
SEND DMAR SIGNAL
DMA
WAS DMA OR INTERRUPT ENABLED ?
554
INTERRUPT
SEND INTERRUPT REG. SIGNAL
558
SEND RECEIVE STATUS TO THE CONTROL REG.
560
DE-ASSERT ACK. SIGNAL WITHIN A TIME SLOT FOR CONNECTIVITY CHECK
562
576
564
YES
CLOCK TRANSITIONS ?
WHAT IS THE SIZE OF THE RECEIVED PACKET ?
256
3
568
566
NO
YES
WAS THE WHOLE PACKET RECEIVED ALREADY ?
NO
CHANGE LINES DOMINATOR TO TRANSMITTER
572
574
4 CYCLES DELAY
570
NO
DOES LINK'S TRANSMITTER HAVE DATA TO TRANSMIT ?
YES
DE-ASSERT ACK. SIGNAL
3
4

Fig. 9B

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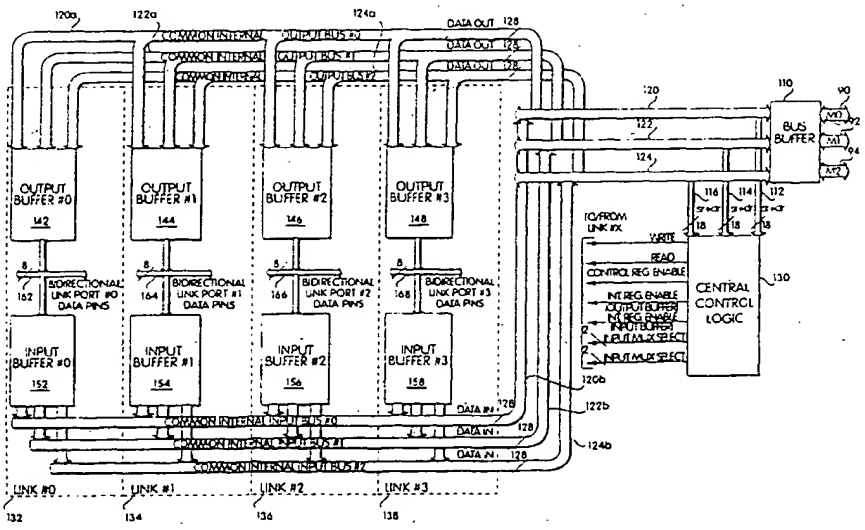

(57) Abstract

A high performance digital signal processor includes a bidirectional communication port for communication with an external device. The bidirectional communication port includes a first transmitting circuit for transmitting to the external device a first clock on a first control line in a transmit mode and for transmitting data words on plural data lines in synchronism with the first clock, and a first receiving circuit for receiving a first acknowledge signal on a second control line in the transmit mode. The communication port further includes a second receiving circuit for receiving a second clock on the second control line in a receive mode and for receiving data words on the data lines in synchronism with the second clock, and a second transmitting circuit for transmitting a second acknowledge signal on the first control line in the receive mode. The communication port further includes switching means for switching between the transmit mode and the receive mode.

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